IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership   Publications/Services   Standards   Conferences   Careers/Jobs

IEEE Xplore™
RELEASE 1.4

Help   FAQ   Terms   IEEE Peer   Quick Links   ▼   » Se
Review

Welcome to IEEE Xplore

○ Home
○ What Can
   I Access?
○ Log-out

Tables of Contents

○ Journals
   & Magazines
○ Conference
   Proceedings
○ Standards

Search

○ By Author
○ Basic
○ Advanced

Member Services

○ Join IEEE
○ Establish IEEE
   Web Account

🖳 Print Format

Your search matched **101** of **787871** documents.
Results are shown **25** to a page, sorted by **publication year** in **descending** order.

You may refine your search by editing the current search expression or entering a new one the te

Then click **Search Again**.

((system <sentence> chip) <or> soc) <sentence> (verify <or> validate)

```
    Search Again
```

Results:
Journal or Magazine = **JNL**   Conference = **CNF**   Standard = **STD**

---

76 **Power analysis and low-power scheduling techniques for embedde software**
Lee, M.T.-C.; Tiwari, V.; Malik, S.; Fujita, M.
System Synthesis, 1995., Proceedings of the Eighth International Symposium

Page(s): 110 -115

[Abstract]   [PDF Full-Text (668 KB)] **CNF**

---

77 **A verification technique for communication hardware and its applic a real chip design**
Fujita, M.; Chen, B.; Yamazaki, M.
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995
Page(s): 619 -622

[Abstract]   [PDF Full-Text (316 KB)] **CNF**

---

78 **APPlaUSE: area and performance optimization in a unified placeme synthesis environment**
Frank, O.; Lengauer, T.
Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 I
International Conference on , 1995
Page(s): 662 -667

[Abstract]   [PDF Full-Text (544 KB)] **CNF**

---

79 **Design and validation with HDL Verilog of a complex input/output for an ATM switch: the CMC**

L Number	Hits	Search Text	DB	Time stamp
-	8	(asic or (system adj3 chip) or (single adj2 chip)) same ((ip or (intellectual property) or (re adj2 usable)) adj3 block)	USPAT; EPO; JPO; IBM_TDB	2002/06/27 11:15
-	8	(asic or (system adj3 chip) or (single adj2 chip)) same ((ip or (intellectual property) or (re adj2 usable)) adj3 block)	USPAT; EPO; JPO; IBM_TDB	2002/06/27 11:18
-	491	user adj interface adj module	USPAT	2002/06/27 11:18
-	1	user adj interface adj module and (netlist adj3 module)	USPAT	2002/06/27 11:27
-	0	user adj interface adj module and (netlist adj3 builder)	USPAT	2002/06/27 11:27
-	0	user adj interface and (netlist adj3 builder)	USPAT	2002/06/27 11:27
-	0	netlist adj3 builder	USPAT	2002/06/27 11:28
-	0	netlist adj3 builder	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/06/27 11:28
-	306	netlist adj3 generat$4	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/06/27 11:29
-	77	(netlist adj3 generat$4) and (gui or (user adj2 interface))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/06/27 11:30
-	8	(netlist adj3 generat$4) and (gui or (user adj2 interface)) and (test adj3 bench)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/06/27 12:47
-	44	(netlist adj3 generat$4) and (gui or (user adj2 interface)) and (verif$3 or verification) and (simulate or simulation)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/06/27 12:49
-	36	((netlist adj3 generat$4) and (gui or (user adj2 interface)) and (verif$3 or verification) and (simulate or simulation)) not ((netlist adj3 generat$4) and (gui or (user adj2 interface)) and (test adj3 bench))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/06/27 12:49
-	1193	((716/4) or (716/5) or (716/17) or (716/18)).CCLS.	USPAT	2002/06/27 15:14
-	174	(((716/4) or (716/5) or (716/17) or (716/18)).CCLS.) and ((user adj3 interface) or gui)	USPAT	2002/06/27 15:14
-	116	((((716/4) or (716/5) or (716/17) or (716/18)).CCLS.) and ((user adj3 interface) or gui)) and parameter$2	USPAT	2002/06/27 15:15
-	25	(((((716/4) or (716/5) or (716/17) or (716/18)).CCLS.) and ((user adj3 interface) or gui)) and parameter$2) and expert	USPAT	2002/06/27 15:15
-	23	((((((716/4) or (716/5) or (716/17) or (716/18)).CCLS.) and ((user adj3 interface) or gui)) and parameter$2) and expert) and (verify or verified or verification or validate$3 or validating)	USPAT	2002/06/27 15:16
-	18	(((((((716/4) or (716/5) or (716/17) or (716/18)).CCLS.) and ((user adj3 interface) or gui)) and parameter$2) and expert) and (verify or verified or verification or validate$3 or validating)) and (asic or pla or fpga or pld or soc or (system adj3 chip))	USPAT	2002/06/27 15:33
-	106000	((system adj3 chip) or soc)	USPAT	2002/08/07 14:08
-	1	((system adj3 chip) or soc) same netlist$3 same (verify or verification)	USPAT	2002/08/07 14:15
-	25	((system adj3 chip) or soc) same netlist$3	USPAT	2002/08/07 14:12
-	109	((system adj3 chip) or soc) and netlist$3 and (verify or verification)	USPAT	2002/08/07 14:34
-	2	(((system adj3 chip) or soc) and (verify or verification)).ti.	USPAT	2002/08/07 14:35
-	7	(((system adj3 chip) or soc) and (verify or verification)).ab.	USPAT	2002/08/08 08:14

C:\APPS\EAST\workspaces\09602422.wsp